A high number of phases enables high frequency techniques and a better thermal management in medium power converters

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ABSTRACT

In this paper, we intend to show that it is possible to obtain advantages in technology selection thanks to the use of the interleaving technique with a very high number of phases. High switching frequency is usually applied to low power converters only, can be used also in medium power converters. It will be seen that there is no penalization in the efficiency and advantages regarding the thermal management can be achieved.

INTRODUCTION

Using interleaving technique [1], a power stage can be divided in several but smaller power stages (named phases), all of them working in parallel. Thus, rms currents are smaller and conduction losses can be reduced. It has been applied in dc-dc converters and power factor correction with few phases (i.e. 2 to 4 phases). With it, medium power converters (200-1000W) are still forced to use typical power MOSFETS (TO-220 or TO-247 case) with large heatsinks. This penalizes the final package and increases the cost. If the same converter is built with a multiphase converter with many phases (tens of phases) new possibilities arise in the selection of the components and different solutions can be obtained.

A good example is the bi-directional dc-dc converter used in dual battery system vehicles that use 14V and 42V batteries. Typically, the power of this converter ranges from 500 to 1000W. The buck converter is suitable for this application due to its simplicity and high efficiency performance (see figure 1). The free wheeling diode of the buck converter has been replaced by a transistor to provide bi-directionality to the converter. Usually, this buck converter is divided in three-to-five paralleled buck stages or phases [2-5], obtaining some advantages especially a filter reduction. Each phase has its own inductor but all of them share the input and the output capacitor.

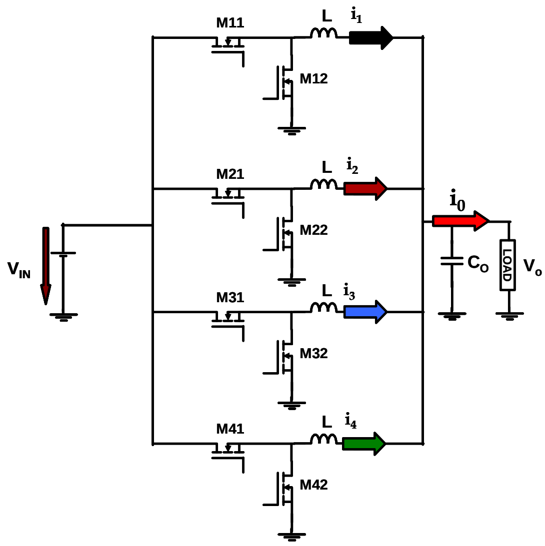


Figure 1.- A multiphase bidirectional buck converter

Our proposal is to use the same technique but with a **very high number of phases**. We have developed two 1000W prototypes: the first is made of 16 phases (figure 2) and the second with 36 (figure 3). The current stress in the semiconductors is greatly reduced and using a different technology becomes a possibility. As can be seen, the power MOSFETs are in a small SO-8 SMD package and inductors are planar (fig. 2) using several PCB layers in parallel. The 36-phases prototype has standard SMD inductors (no custom made) and a very small output capacitor (fig. 3).

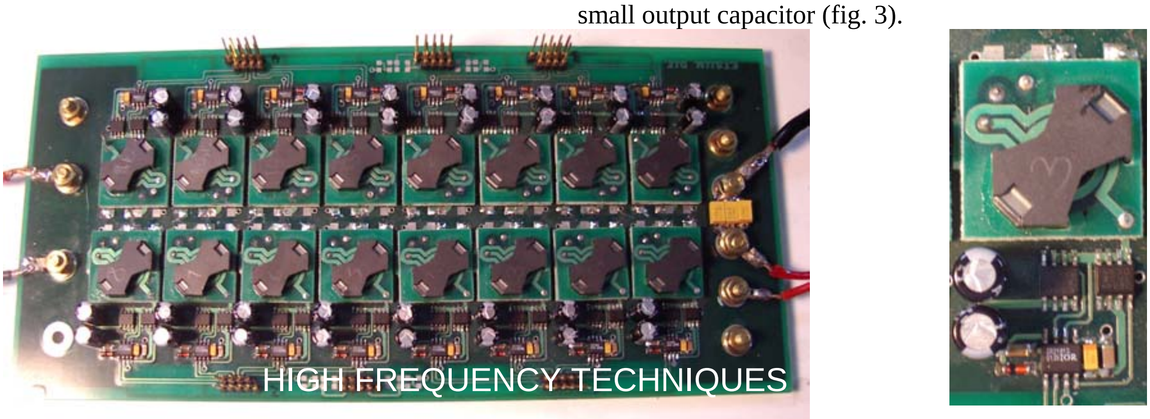


Figure 2.- A 1000W 16-phases bidirectional buck converter (left side) and a single phase(right side)

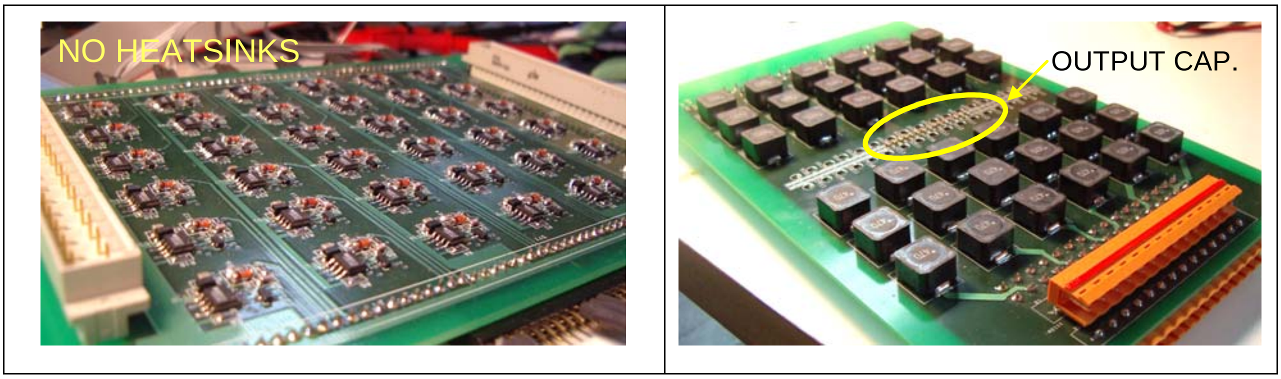


Figure 3.- A 1000W 36-phases bidirectional buck converter: semiconductor layer (left side) and output filter layer (right)

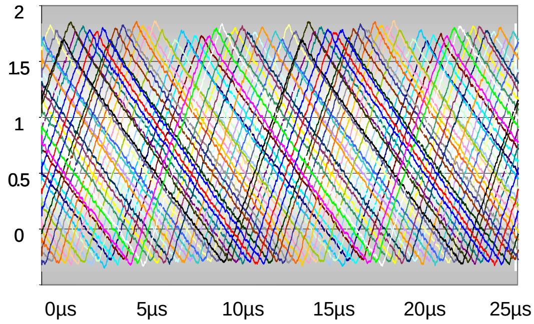
Among the advantages, the thermal management is the most important. Since the focus of the power losses is spread, no heatsinks are required. In addition to that, the output filter is very small taking advantage of the interleaving technique with many phases. As a conclusion, low power techniques can be applied to medium and high power converters and it opens new possibilities.

TIPS AND EXPERIMENTAL RESULTS

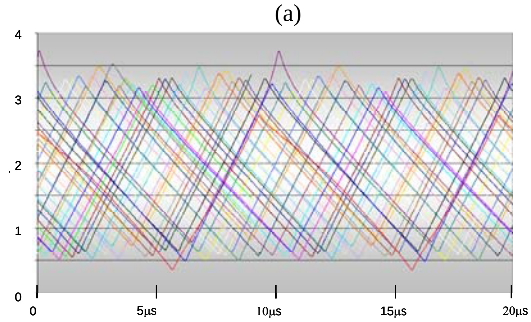
This type of designs, with such a high number of phases creates new problems that should be overcome: how to drive so many transistors and how to balance the phase currents. In principle, commercial ICs for multiphase converters are not valid since they only drive up to four phases [6]. However, due to the renewed interest in multiphase converters, companies start to show new products able to drive more phases. In particular, a DSP based solution [7] can drive 16 phases with very high resolution.

In general, these multiphase circuits should be driven by a digital device. In our case, both circuits were controlled by a FPGA. It is very easy to generate many delayed gate signals (DPWM) with small silicon area [8]. The cost of these digital devices (FPGA and DSP) has dropped very fast in last years and the cost is very competitive. Moreover, some of the required hardware such as ADCs is usually included. Finally, it should be remarked that the each driver must be placed close to each power transistor being possible to place the FPGA in a different layer. Therefore, the layout is a little bit more complex than a classical converter.

The second problem (possible current unbalance) is also minimized by the use of the digital control. The main reason for dc current mismatches is duty unbalance [9]. The high accuracy of the DPWM solves this problem in many of the cases without using current loops. Figure 4 shows the measured phase currents in the 36-phases prototype without using current loops (at 100 and 80kHz). At full load, the phase with the maximum dc current only exceeds 10% the average value. It should be noted that the positive temperature coefficient of the Rdson resistance of the MOSFETs helps a lot in reaching the equilibrium. At least, for this application with 60V MOSFETs and using a digital controller, no current loops are required. In other applications such as VRM, with smaller Rdson MOSFETs, the steady-state may show a worse equilibrium. This unbalance is kept constant even during transient conditions. Figure 5 shows four phases running under a load step. It can be seen that all of them have the same shape.



(a)



(b)

Figure 4.- Experimental results from the 36-phases prototype: (a) current waveforms at half-load; (b) current waveforms at full-load

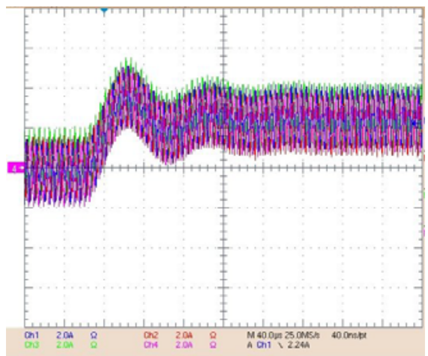


Figure 5.- Current waveforms of 4 phases under a load step (2A/div) and (10µs/div)

Figure 6 shows the efficiency measurements of both circuits including the drivers (3W in the 16-phases prototype and 1.2W in the 36-phases). Efficiency reaches 95% for the 16-phases circuit at full load. Slightly smaller values have been obtained in the 36-phases prototype although similar efficiency is showed at 700W (94%).

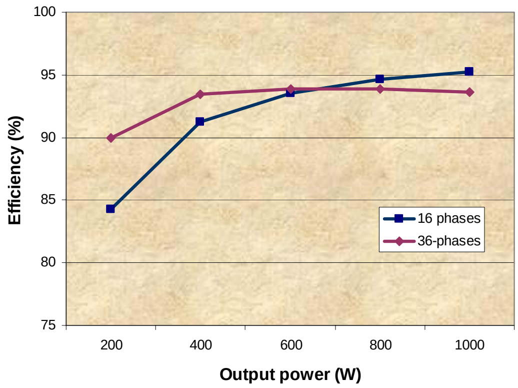


Figure 6.- Measured efficiency of both prototypes including the driver stage

One of the advantages of the multiphase converters is ripple cancellation [10]. Ideally, and depending on the duty cycle, output current ripple can be very small, obtaining big reductions in the output capacitor. Not only the ripple is smaller, but also its frequency is higher. Figure 7 shows the cancellation factor (coefficient that should be multiplied by the actual phase current ripple to obtain the total output current ripple) as a function of the duty cycle for several number of phases. This concept is especially advantageous with a very high number of phases because ripple cancellation is high and much less sensitive to duty cycle variations. With 16 phases, current ripple is zero for sixteen different duty cycles and, among them, the cancellation is very high (smaller than 0.1). Therefore, a small output capacitor is expected.

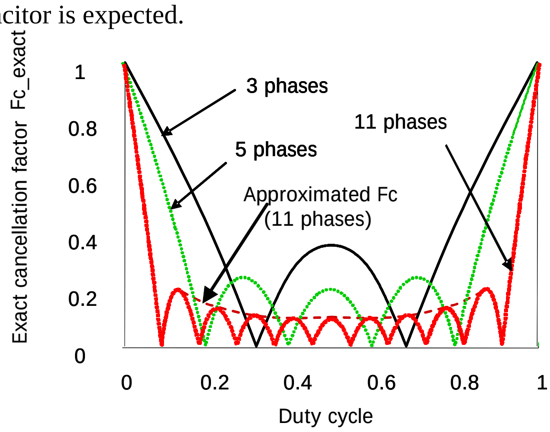


Figure 7.-Ripple cancellation factor as a function of the duty cycle for several number of phases

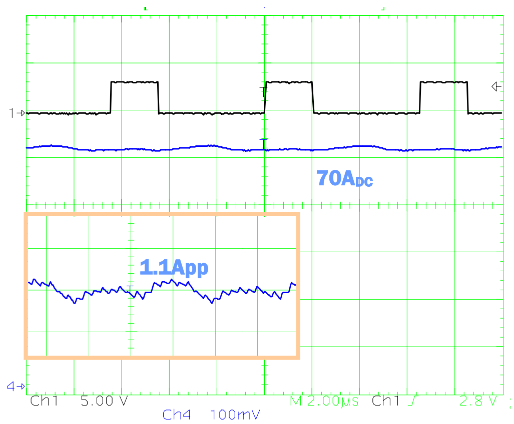


Figure 8.- Gate signal of one phase and total output current (10A/div); detail of output current ripple (1A/div) with (2µs/div) in the 16-phases prototype

Figure 8 shows the output current of the 16-phases converter without output capacitor (this is the addition of all the inductor currents). It can be seen that over 70A dc current, there is a small current ripple (1.1 A peak to peak), easy to be filtered requiring a small capacitor. In the second prototype (36-phases) the output capacitor is even smaller (see table I).

Once digital control is adopted, new advantages arise. Especially important for multiphase converter is the capability to switch on/off depending on the load. It is very easy to improve the efficiency of the converter at light load (not implemented in this experiment). Figure 9 shows an example of the efficiency improvement using this technique in the 16-phases circuit. At light load, up to 20W can be saved.

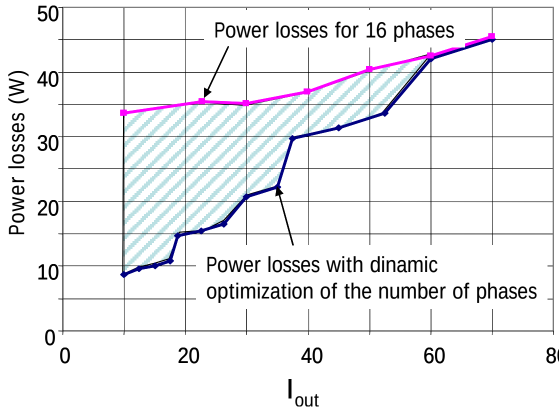


Figure 9.- Power savings in the 16 prototype

COMPARISON OF DESIGNS

Table I shows a comparison among several designs for the automotive 42/14V bi-directional converter. Single phase design is theoretical; state of the art columns are taken from [3-4] (data between brackets are estimations); finally, last two columns with the proposed designs have been included. All of these circuits were designed for 1000W. Some conclusions can be obtained from table I:

- The higher the number of phases, the smaller the MOSFET size. A high number of phases allows the use of SMT transistors. Moreover, with a proper design heatsinks can be avoided. The heat generated in the silicon is not concentrated in few devices; on the contrary, the heat is spread along the PCB.
- Same can be said about the inductors, obtaining a small size for the second design. Even with 36 phases, the total inductor volume is smaller compared with the others designs (see row 8 of the table). The use of planar or SMT inductors is highly recommended to increase reliability and repetitiveness.
- Output capacitance: with 16 interleaved phases, there is a very high ripple cancellation for every duty cycle. However, the tolerances in the inductance forces to use a relative large output capacitor (authors do not know if the previous works shown in columns 2 and 3 have considered this phenomenon). This effect is much smaller in the 36 phases converter where a small filter is obtained. In these designs, the output capacitors have been adjusted by experiment to obtain 1% voltage ripple.

		Theoretical	State of the Art		Proposed designs	
	Name of design	**-**	**[3]**	**[4]**	**Design 1**	**Design 2**
	Number of phases	**1**	**3**	**5**	**16**	**36**
1	**Output power (W)**	1000	1000	1000	1000	1000
2	**Power per phase (W)**	1000	333	200	62	28
3	**Switching freq. (kHz)**	100	150	82	150	100
4	**MOSFET per phase**	6 x SUP75N08	2 x (??)	2 x SUP75N08	2 x SI4450	1 x IRF7341
5	**MOSFET case**	6 x TO247	2 x (TO247)	2 x D2PAK	2 x SO-8	1 x SO-8
6	**Inductor core**	4 x RM14	RM14	RM10	RM7	WE PD-47
7	**Inductor height (mm)**	30.0	30.0	18.6	13.4	10.0
8	**Total inductor vol. (cm^3)**	144.4	108.3	56.7	63.4	36.2
9	**Output capacitance (µF)**	144	75	47	99	12
10	**Avg phase current (A)**	71.2	23.8	14.2	4.4	2.0
11	**Phase current ripple (%)**	7	100	104	220	100
12	**Heatsinks**	Yes	Yes	Yes	No	No
13	**Control stage**	Any analog IC	Spec. analog IC	Spec. analog IC	Digital	Digital
14	**Current sharing**	Not applicable	Current loops	Current loops	Passive	Passive
15	**Efficiency full load (%)**	92	88	93	95	93

Table I.- Summary of the main features of the developed converters versus the state of the art

- Two differential features are common to these two designs: first, they do not use commercial IC to control but specific circuits using digital devices; second, no heatsinks are used in them. This is one of the most important differences because it simplifies the constructive process and reduces the manufacturing cost.
- Efficiency in the proposed designs is very high and very competitive with the designs with less number of phases. Therefore, it can be said that this type of technique does not penalize the efficiency of the converter.
- Designing with many phases requires more board space and a more complex layout. On the other hand, the height of the components is much smaller. This fact together with the absence of heatsinks forces to design in a different way the mechanical part of the converter.

CONCLUSIONS

Medium power converters can be designed using many small converters (phases) running in parallel. Since the power managed by each phase is a fraction of the total, small SMD components can be used and high frequency techniques can be used.

Thermal management improvement is probably the major advantage of this approach. Since the efficiency is high and the heat is not concentrated in few devices, heatsinks can be removed reducing the manufacturing cost.

The layout of the converter should be designed carefully, paying attention to the position of the drivers and the power transistors. More board space is required but less height, being possible to build low profile converters.

Last but not least, digital control is mandatory to obtain the proper delay of the gate signals and to avoid current unbalance.

REFERENCES

[1] B.A. Miwa, D.M. Otten, M.E. Schlecht, M.E., “High efficiency power factor correction using interleaving techniques” IEEE Applied Power Electronics Conference and Exposition, 1992 (APEC '92).

[2] J. Czogalla, J. Li, C.R. Sullivan, “Automotive application of multi-phase coupled-inductor DC-DC converter”, Industry Applications Conference, 2003, Vol. 3 , pp. 1524 – 1529.

[3] A. Consoli, G. Scarcella, G. Giannetto, A. Testa, “A multiphase DC/DC converter for automotive dual voltage power systems”, PCIM 2001.

[4] T.C. Neugenbauer, D.J. Perrault, “Computer Aided Optimization of DC/DC Converters for Automotive Applications”, IEEE Transactions on Power Electronics, Vol.18, No.3, May 2003.

[5] M. Gerber, J.A. Ferreira, I.W. Hofsaer, N. Seliger, “Interleaving Optimization in Synchronous Rectified DC/DC Converters”, IEEE Power Electronics Specialists Conference 2004 (PESC04).

[6] TPS40090, "High-Frequency Multiphase Controller", Texas Instrument Datasheet, Oct. 2003.

[7] TMS320F28044, "Digital Signal Processor", Texas Instrument Datasheet, May 2007.

[8] O. Garcia, P. Zumel, A. de Castro, J.A. Cobos, “Automotive dc-dc bidirectional converter made with many interleaved buck stages”, IEEE Transactions on Power Electronics, Vol. 21, No. 3, págs. 578-586.

[9] A. V. Peterchev, J. Xiao, S. R. Sanders, “Architecture and IC Implementation of a Digital VRM Controller”, IEEE Trans. on Power Electronics, vol. 18, no. 1, Jan. 2003.

[10] W. Chen, “High efficiency, high density, polyphase converter for high current applications”, Linear Technology Application note 77, September 1999.